WHAT IS CLAIMED IS:

1. A three-dimensional circuit comprising a plurality of stacked levels on a substrate, each level comprising a plurality of all-metal circuit components exhibiting giant magnetoresistance and arranged in two dimensions, the circuit further comprising an interconnect for providing interconnections between the circuit components on different ones of the plurality of levels.

2. The circuit of claim 1 wherein the plurality of circuit components on at least one of the levels comprise a plurality of memory cells, each memory cell comprising a multi-layer structure exhibiting magnetoresistance.

3. The circuit of claim 2 wherein each multi-layer structure comprises:

a plurality of magnetic layers, at least one of the magnetic layers being for magnetically storing one bit of information;

a plurality of the access lines integrated with the plurality of magnetic layers and configured such that the bit of information may be accessed using selected ones of the plurality of access lines and the giant magnetoresistive effect; and

at least one keeper layer;

wherein the magnetic layers, the access lines, and the at least one keeper layer form a substantially closed flux structure.

4. The circuit of claim 2 further comprising a semiconductor level among the plurality of stacked levels.

5. The circuit of claim 4 wherein the substrate comprises the semiconductor level.

6. The circuit of claim 4 wherein the semiconductor level comprises support electronics for controlling access to the plurality of memory cells.

7. The circuit of claim 2 wherein the plurality of memory cells are arranged in a plurality of substantially identical and interchangeable memory array modules.

8. The circuit of claim 7 wherein each memory array module further comprises all-metal support electronics for controlling access to the corresponding memory array module.

9. The circuit of claim 7 wherein the memory array modules are arranged in the two dimensions and stacked to form at least a portion of the stacked levels of all-metal circuit components.

10. The circuit of claim 7 further comprising all-metal support electronics for controlling access to the plurality of memory cells.

11. The circuit of claim 10 wherein the all-metal support electronics are arranged in a plurality of circuit modules which are arranged in the two dimensions and stacked with the memory array modules to form at least a portion of the stacked levels of all-metal circuit components.

12. The circuit of claim 2 wherein the plurality of circuit components on at least one other one of the levels comprise all-metal support electronics for controlling access to the plurality of memory cells.

13. The circuit of claim 12 wherein the plurality of the memory cells and the all-metal support electronics are arranged on separate ones of the stacked levels.

14. The circuit of claim 12 wherein the plurality of the memory cells and the all-metal support electronics are combined on selected ones of the stacked levels.

15. The circuit of claim 1 wherein the plurality of circuit components on at least one of the levels comprise a plurality of active circuit components, each active circuit component operable to generate an output signal based on the giant magnetoresistive effect.

16. The circuit of claim 15 wherein at least one of the active circuit components comprises a transpinnor comprising a network of multi-layer thin-film elements, at least one thin-film element in the transpinnor exhibiting giant magnetoresistance, the transpinnor further comprising a conductor magnetically coupled to the at least one thin-film element for controlling operation of the transpinnor, wherein the transpinnor is operable to generate an output signal which is a function of a resistive imbalance among the thin-film elements and which is proportional to a power current in the network of thin-film elements.

17. The circuit of claim 15 wherein the active circuit components are interconnected to form a plurality of circuit modules.

18. The circuit of claim 17 wherein the circuit modules are arranged in the two dimensions and stacked to form at least a portion of the stacked levels of all-metal circuit components.

19. The circuit of claim 1 wherein the interconnect comprises a plurality of intra-level interconnect structures, each corresponding to one of the stacked levels and providing first connections among the circuit components on the corresponding level, the interconnect further comprising at least one inter-level interconnect structure for providing second connections among the intra-level interconnect structures.

20. The circuit of claim 19 wherein the at least one inter-level interconnect structure comprises a plurality of inter-level interconnect structures each of which provides a portion of the second connections between selected ones of the intra-level interconnect structures.

21. The circuit of claim 1 wherein the substrate comprises any of a semiconductor, a metal, and a dielectric.

22. An electronic system comprising the circuit of claim 1.

23. A memory system comprising a plurality of stacked levels on a substrate, each level comprising a plurality of all-metal memory cells arranged in two dimensions, each memory cell comprising a multi-layer structure exhibiting magnetoresistance, the structure further comprising support electronics and an interconnect for controlling access to the memory cells.

24. A three-dimensional circuit comprising a plurality of stacked levels on a substrate, each level comprising a plurality of all-metal circuit components exhibiting giant magnetoresistance and arranged in two dimensions, the circuit components forming logic and processing circuitry, the circuit further comprising an interconnect for providing interconnections between the circuit components on different ones of the plurality of levels.

25. A three-dimensional circuit comprising a plurality of stacked levels on a substrate, each level comprising a plurality of all-metal circuit components exhibiting giant magnetoresistance and arranged in two dimensions, the circuit components forming linear analog circuitry, the circuit further comprising an interconnect for providing interconnections between the circuit components on different ones of the plurality of levels.

26. A system-on-a-chip, comprising a three-dimensional circuit comprising a plurality of stacked levels on a substrate, each level comprising a plurality of all-metal circuit components exhibiting giant magnetoresistance and arranged in two dimensions, the circuit components comprising a plurality of all-metal memory cells, each memory cell comprising a multi-layer structure exhibiting magnetoresistance, the circuit components further comprising support electronics for controlling access to the memory cells, logic and processing circuitry, and linear analog circuitry, the circuit further comprising an interconnect for providing interconnections between the circuit components on different ones of the plurality of levels.

27. A memory system, comprising a plurality of stacked levels on a substrate, each of first selected ones of the stacked levels comprising a plurality of all-metal memory

cells arranged in two dimensions, each memory cell comprising a multi-layer structure exhibiting magnetoresistance, each multi-layer structure comprising a plurality of magnetic layers at least one of which is operable to magnetically storing one bit of information, and a plurality of the access lines integrated with the plurality of magnetic layers and configured such that the bit of information may be accessed using selected ones of the plurality of access lines and the giant magnetoresistive effect, wherein the magnetic layers and the access lines are part of a substantially closed flux structure, and wherein second selected ones of the stacked levels comprise support electronics for facilitating access to the memory cells, the support electronics comprising a plurality of active circuit components, each active circuit component comprising a network of multi-layer thin-film elements at least one of which is operable to exhibit giant magnetoresistance, and a conductor magnetically coupled to the at least one thin-film element for controlling operation of the transpinnor, wherein each active circuit component is operable to generate an output signal which is a function of a resistive imbalance among the thin-film elements and which is proportional to a power current in the network of thin-film elements.

28. The memory system of claim 27 wherein selected ones of the plurality of memory cells form blocks of memory, the selected memory cells corresponding to each block of memory forming vertical stacks in consecutive ones of the stacked layers.

29. A three-dimensional circuit comprising a plurality of stacked levels on a substrate, each level comprising a plurality of circuit modules having substantially identical dimensions arranged in a contiguous, two-dimensional array, each circuit module comprising a plurality of all-metal circuit components, the circuit further comprising a level

interconnect for providing interconnections between the circuit modules on different ones of the plurality of stacked levels.

30. The circuit of claim 29 wherein the circuit components comprise memory cells, each memory cell comprising a multi-layer structure exhibiting magnetoresistance.

31. The circuit of claim 30 wherein each multi-layer structure comprises:

a plurality of magnetic layers, at least one of the magnetic layers being for magnetically storing one bit of information; and

a plurality of the access lines integrated with the plurality of magnetic layers and configured such that the bit of information may be accessed using selected ones of the plurality of access lines and the giant magnetoresistive effect;

wherein the magnetic layers and the access lines are part of a substantially closed flux structure.

32. The circuit of claim 31 wherein each multi-layer structure further comprises at least one keeper layer which is part of the substantially closed flux structure.

33. The circuit of claim 29 wherein the circuit components comprise active circuit components, each active circuit component being operable to generate an output signal based on the giant magnetoresistive effect.

34. The circuit of claim 33 wherein the active circuit components comprise transpinnors, each transpinnor comprising a network of multi-layer thin-film elements, at least one thin-film element in the transpinnor exhibiting giant magnetoresistance, the

transpinnor further comprising a conductor magnetically coupled to the at least one thin-film element for controlling operation of the transpinnor, wherein the transpinnor is operable to generate an output signal which is a function of a resistive imbalance among the thin-film elements and which is proportional to a power current in the network of thin-film elements.

35. The circuit of claim 29 wherein the plurality of circuit modules comprise substantially identical and interchangeable memory array modules.

36. The circuit of claim 35 wherein each memory array module comprises an array of all-metal memory cells.

37. The circuit of claim 36 wherein each memory array module comprises all-metal support electronics operable to facilitate access to the array of memory cells.

38. The circuit of claim 37 wherein the memory cells and the support electronics are deployed in separate layers of the memory array module.

39. The circuit of claim 37 wherein the memory cells and the support electronics are deployed in a single layer of the memory array module.

40. The circuit of claim 36 wherein each memory array module comprises a module interconnect for facilitating connections within the memory array module and for connecting to the level interconnect.

41. The circuit of claim 35 wherein the substrate comprises a semiconductor substrate.

42. The circuit of claim 41 wherein the semiconductor substrate comprises support electronics for facilitating access to the memory array modules.

43. The circuit of claim 35 wherein each of the memory array modules comprises an array of nonvolatile memory cells and is operable to function independently.

44. The circuit of claim 43 wherein access to the memory cells in a particular memory array module requires power to be applied only to the particular memory array module.